

FIG.1

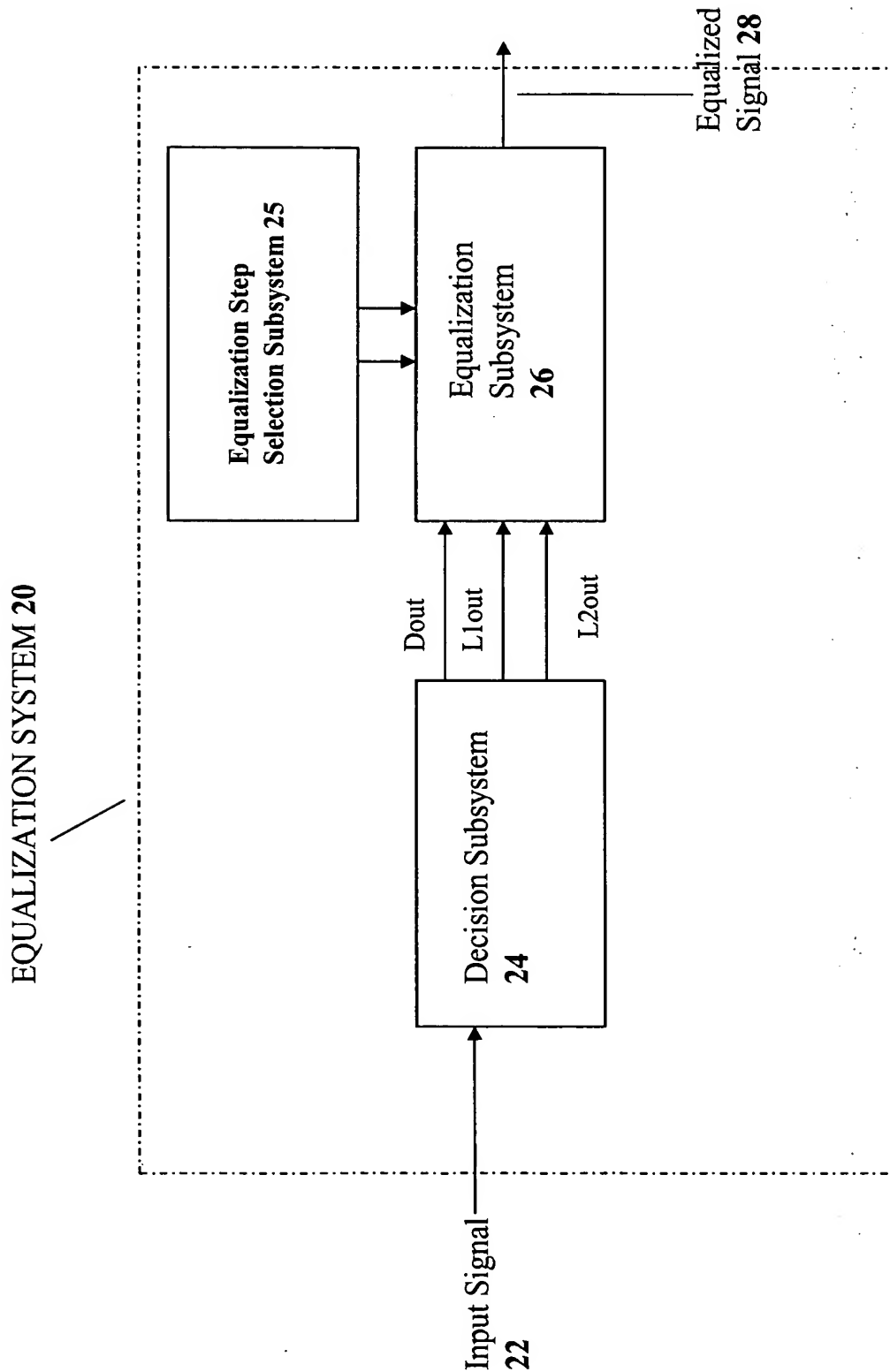


Fig. 2

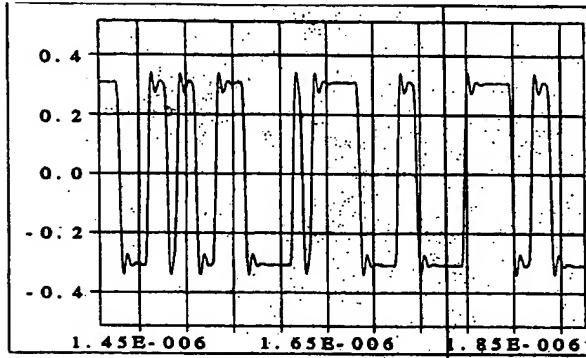


Fig. 3(a)

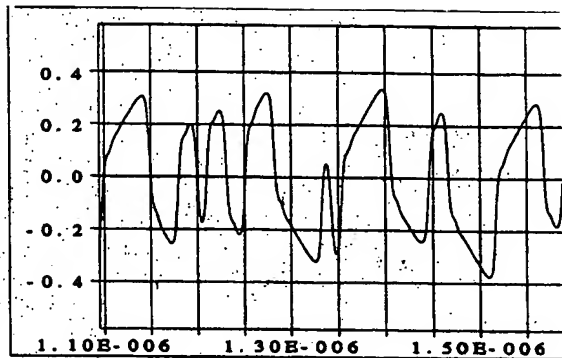


Fig. 3(b)

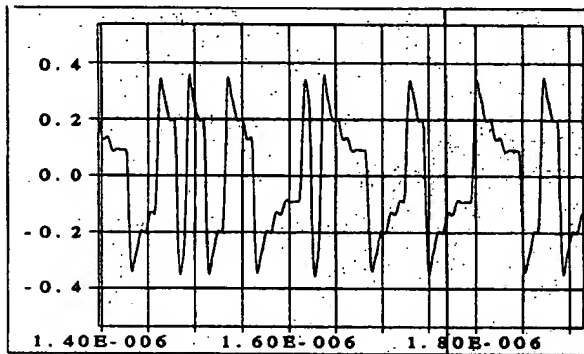


Fig. 4(a)

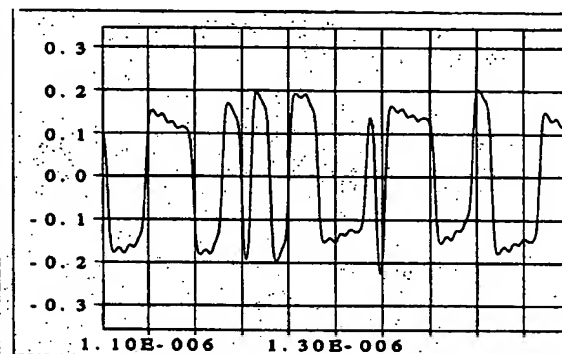


Fig. 4(b)

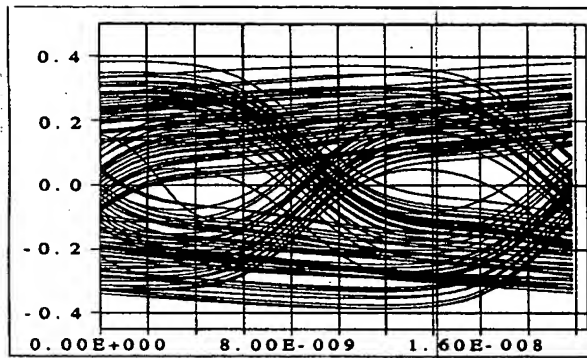


Fig. 5(a)

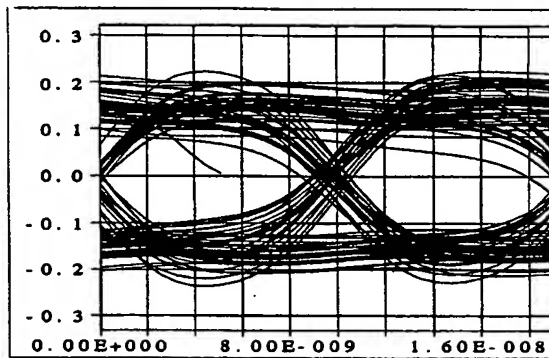


Fig. 5(b)

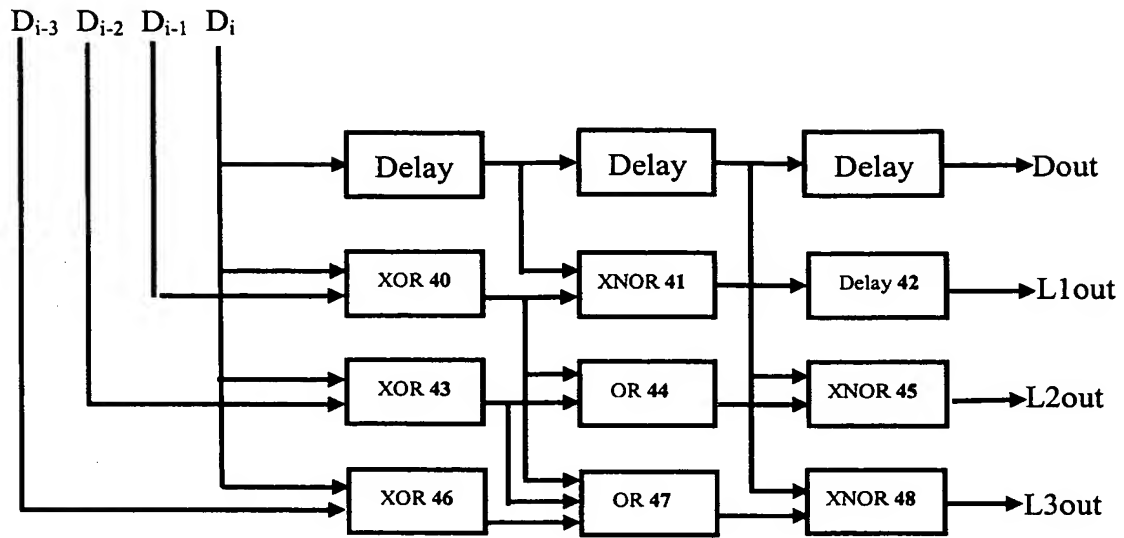


Fig. 6 A block diagram for the equalization logic that generates the three signals levels

Sample Input Stream = 01000111100 (a = MSB; b = first to right of MSB; k = LSB)
 a = 0; b = 1; c = 0; d = 0; e = 0; f = 1; g = 1; h = 1; i = 1; j = 0; k = 0

Bit Identity	Dout	L1out	L2out	L3out
a	0	-----	-----	-----
b	1	1	1	1
c	0	0	0	0
d	0	1	0	0
e	0	1	1	0
f	1	1	1	1
g	1	0	1	1
h	1	0	0	1
i	1	0	0	0
j	0	0	0	0
k	0	1	0	0

Fig. 7

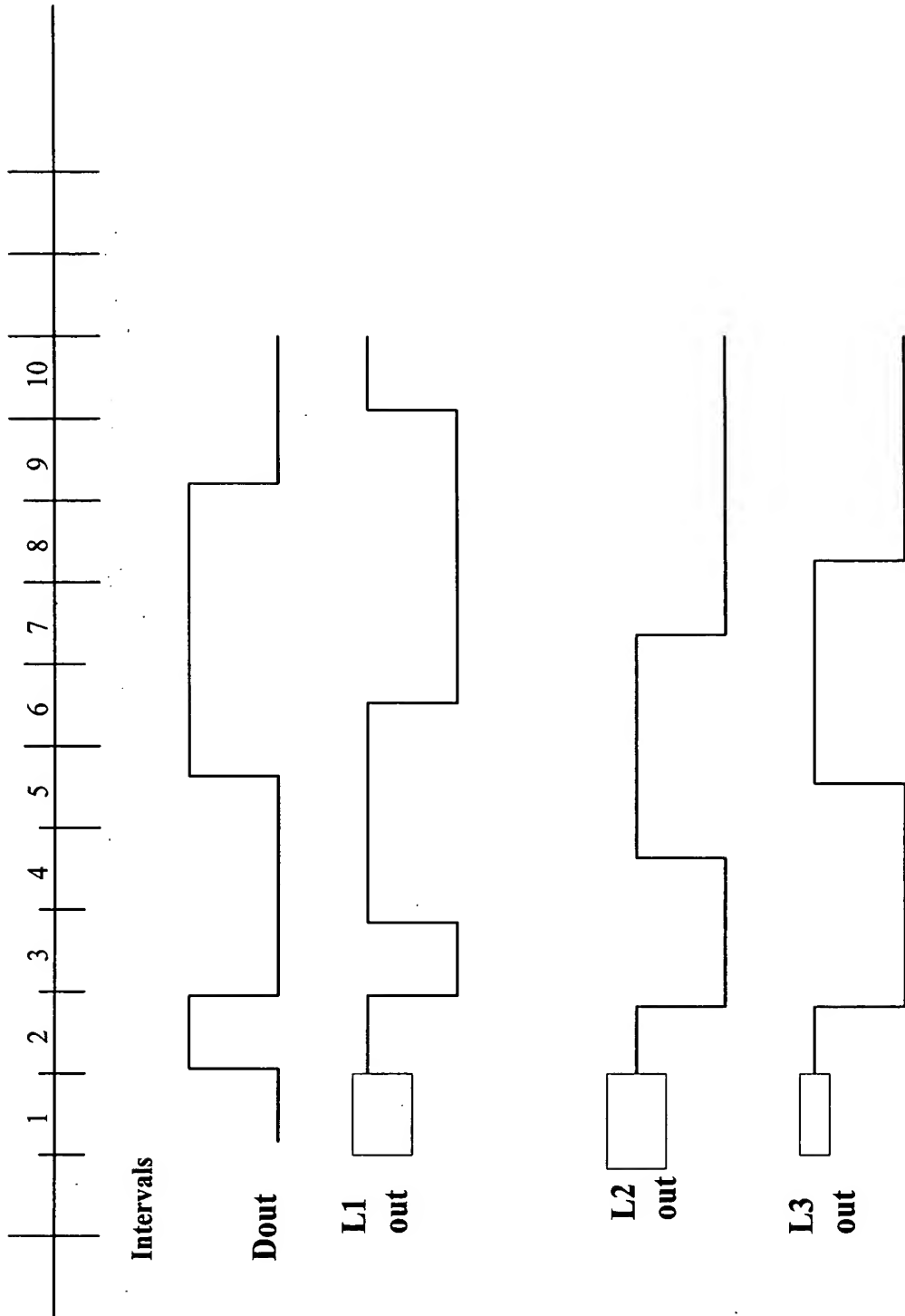


Fig. 8

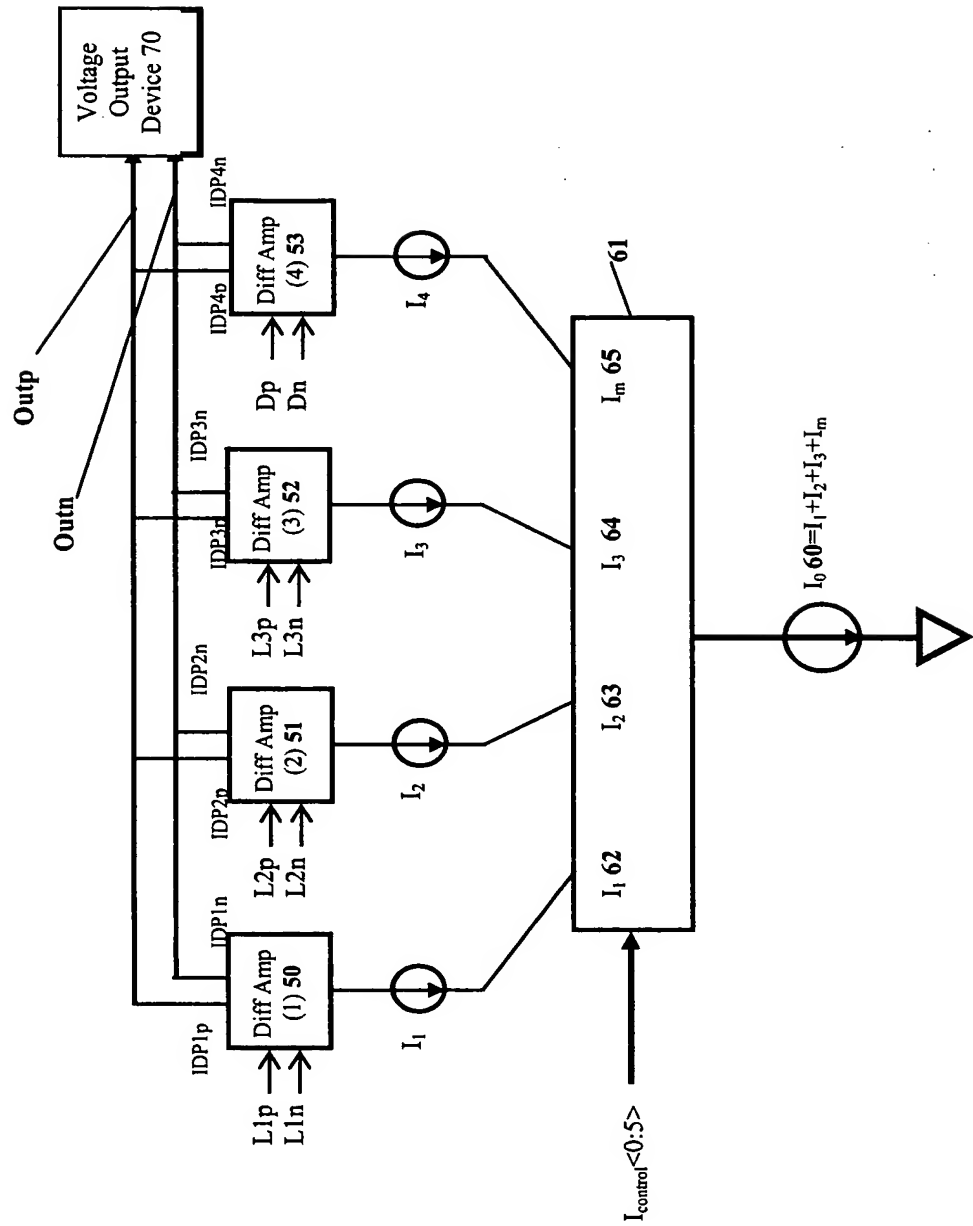


Fig.9

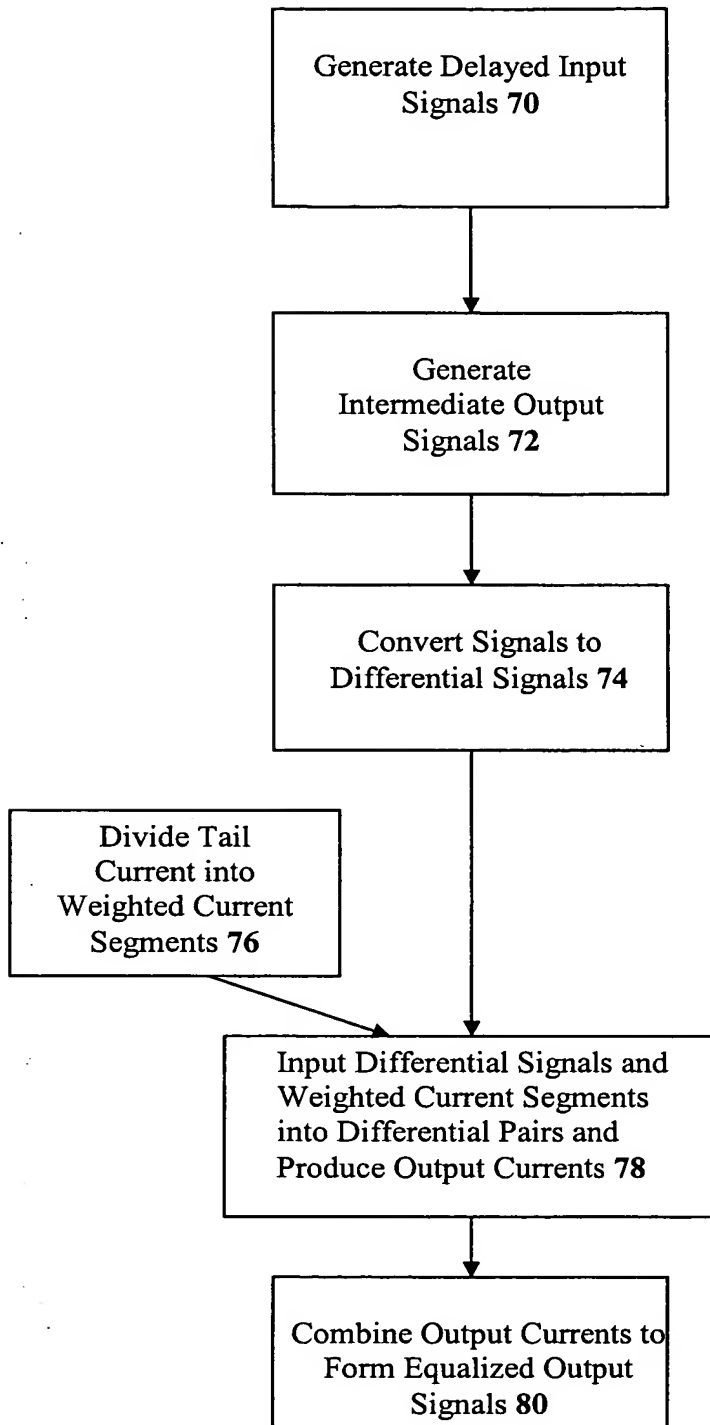


Fig. 10